

Intel® Architecture Enhancements for the Enterprise

Robert Yung, Ph.D.

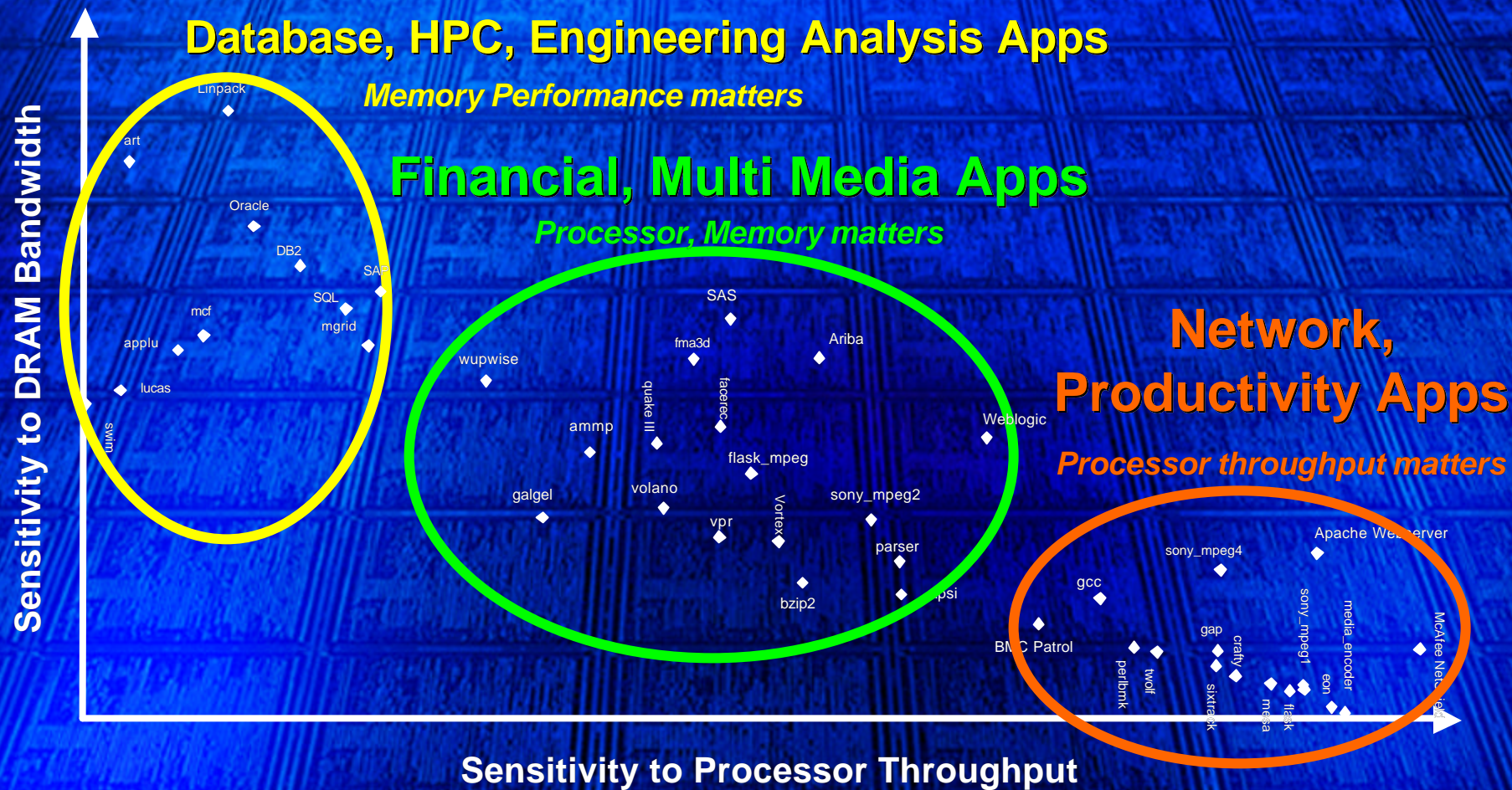
**Chief Technology Officer
Enterprise Processors
Intel Corporation**

October 15, 2002



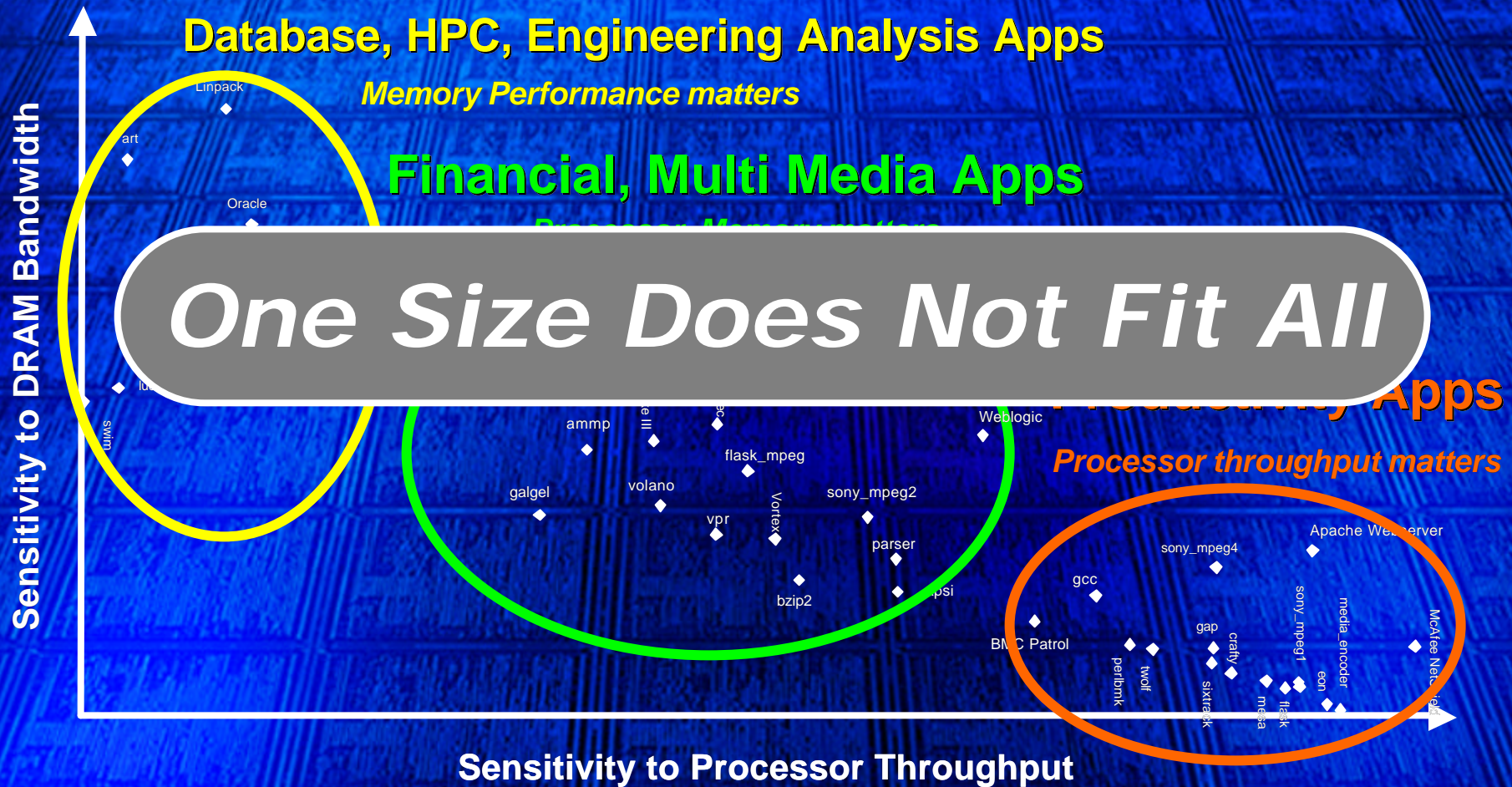
Processor, Memory Sensitivity of Apps

Some Examples



Apps Show Different Sensitivity To Memory, Processor Throughput

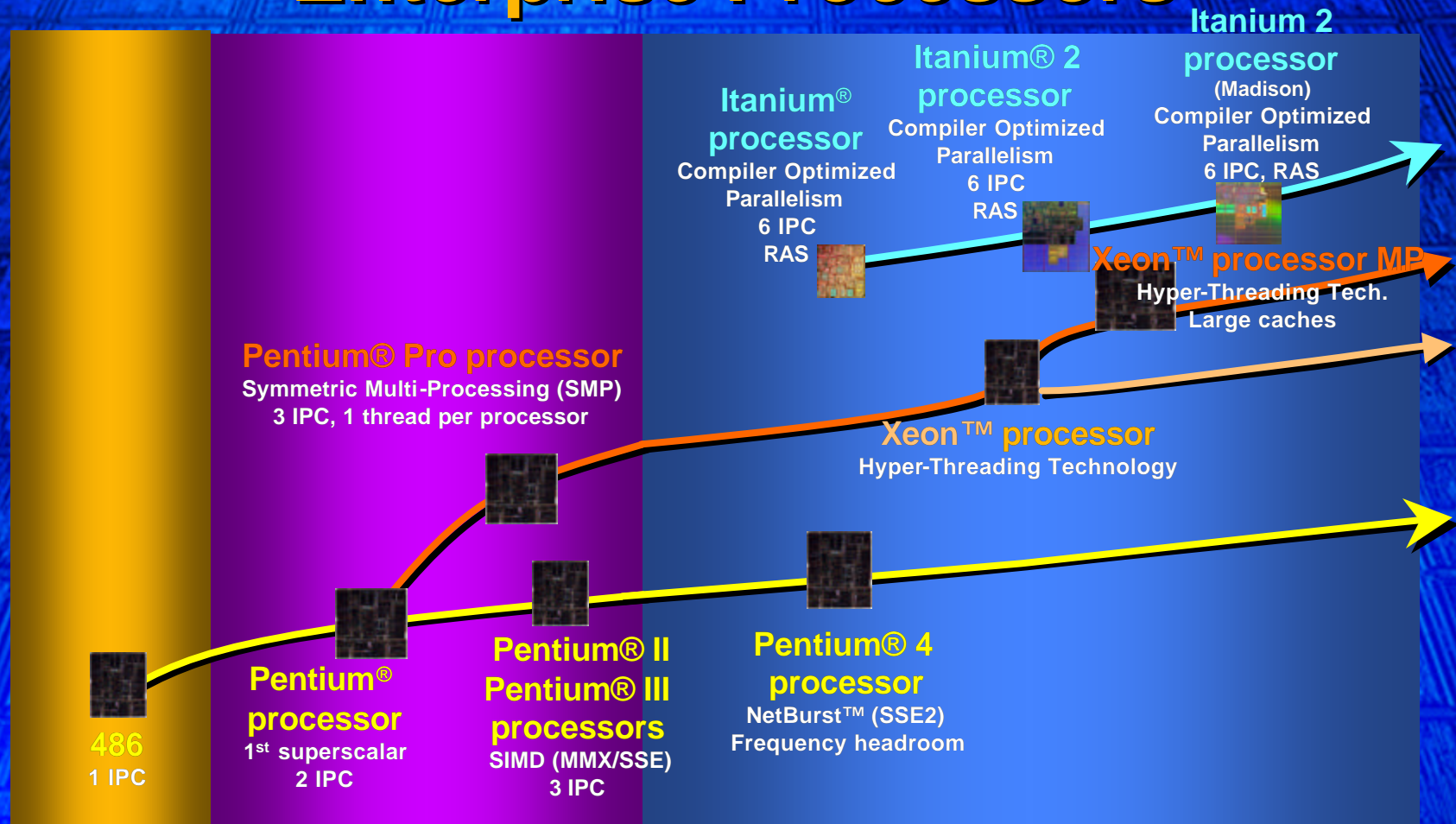
Processor, Memory Sensitivity of Apps



Apps Show Different Sensitivity To Memory, Processor Throughput

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Evolution of Intel® Architecture Enterprise Processors



Future: Rich Multi-threading (N-cores, M-threads), More Caches, Faster Interconnects, App-/System-optimized Performance, RAS-enhancements

Intel® Architecture Enterprise Server Roadmap

2002

2003

2004



**Itanium® 2
Processor**
(McKinley **3MB iL3***)

**Itanium® 2
Processor**
(Madison/Deerfield
up to **6MB iL3***)

Montecito
(**>6MB iL3***)

**Xeon™
Processor MP**
(**1MB iL3**)

**Xeon™
Processor MP**
(**>1MB iL3****)

**Xeon™
Processor MP**

Full Platform
Compatibility



**Xeon™
Processor**
(**512KB iL2,
400/533** FSB**)

**Xeon™
Processor**

**Silicon
Process**

0.18 µm

0.13 µm

90 nm

*Maximum Cache

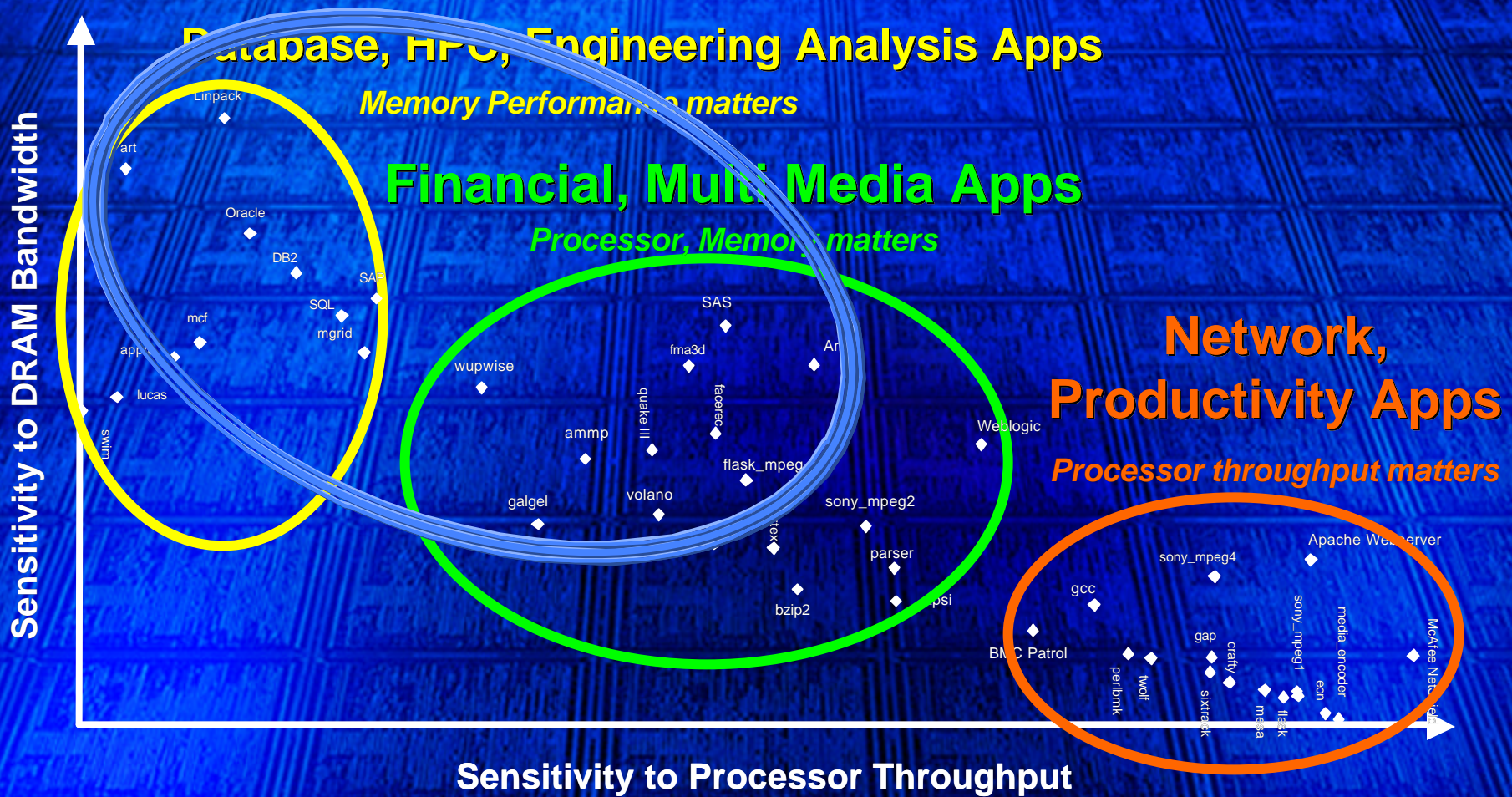
**Future product

intel

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Itanium® Processor Family Design Sweet Spots

A Snapshot



Focus: Large Memory, Data Bandwidth, RAS

Itanium® Processor Family Design Sweet Spots

A Snapshot

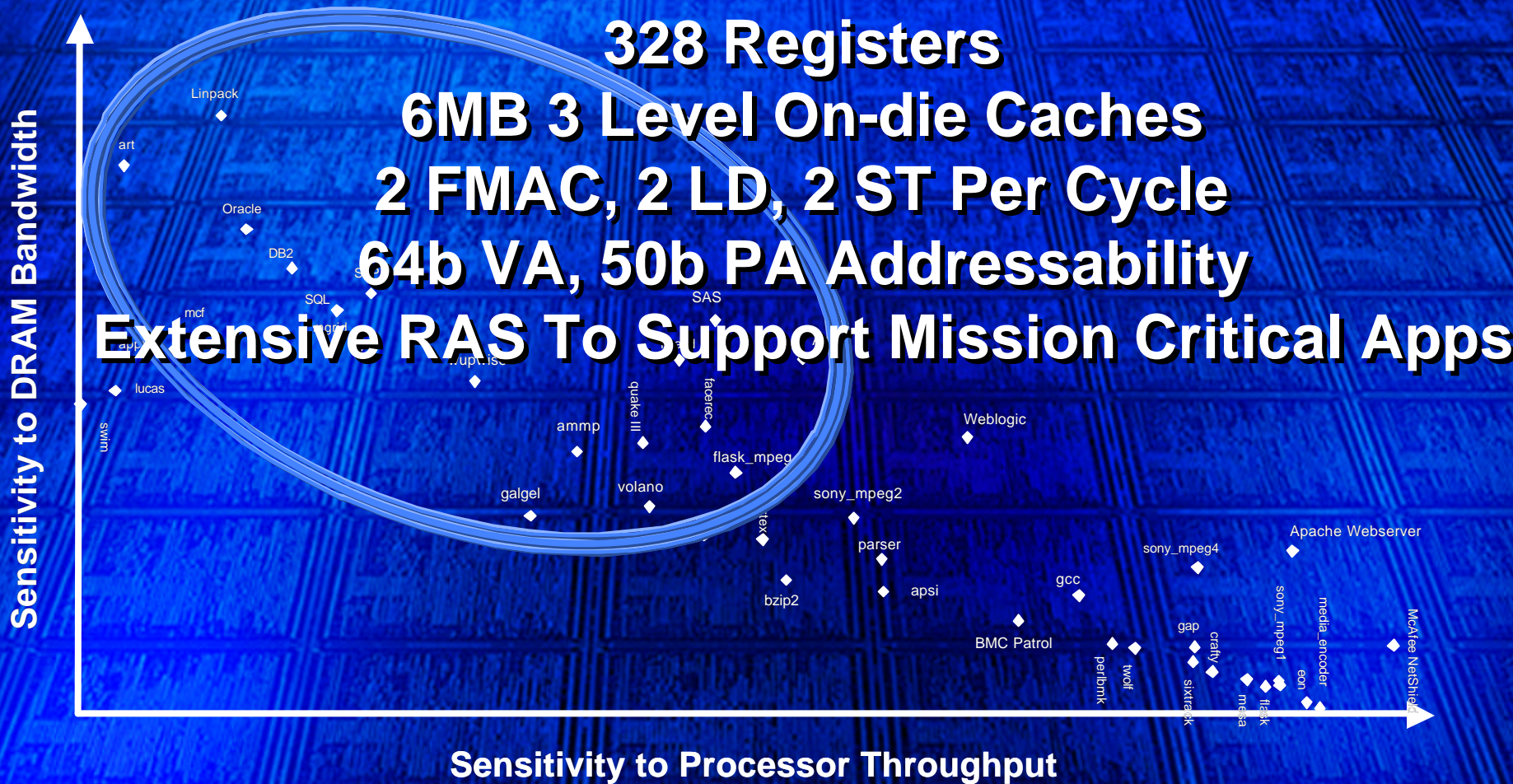
328 Registers

6MB 3 Level On-die Caches

2 FMAC, 2 LD, 2 ST Per Cycle

64b VA, 50b PA Addressability

Extensive RAS To Support Mission Critical Apps



Focus: Large Memory, Data Bandwidth, RAS

Itanium® 2 Processor

Record Setting Performance



BENCHMARK	SAP (2 Tier) ¹ Sales and Distribution	TPC-C ² Transaction Processing	Linpack ³ High Performance Computing	TPC-C ⁴ Transaction Processing	Stream ⁵ Platform Bandwidth
SCALE	4-way	4-way	32-way	32-way	64-way
RESULT	470 USERS	78.4K tpmC	101 GFLOPS	308K tpmC	120 GB/sec
30-50% performance improvement expected with Madison					
	\$5.11 per tpmC		\$14.96 per tpmC		
	WORLD RECORD	WORLD RECORD	WORLD RECORD	IA SMP RECORD	WORLD RECORD

1 Source: Itanium® 2 processor results measured on HP Server rx5670 using 4 Itanium® 2 processors 1GHz with integrated 3MB L3 cache, 16GB of memory, Windows Advanced Server LE 1.2, SAP rev 4.6 C, SQL Server Enterprise Edition 64bit.

2 Source www.tpc.org: Itanium® 2 processor measurements done on a HP Server rx5670 using 4 Itanium® 2 processors 1GHz with integrated 3MB L3 cache, 48GB memory, Windows Advanced Server LE 1.2, SQL Server Enterprise Edition 64bit, availability date 12/31/02.

3 Source: Itanium® 2 processor measurements done on a NEC Server TX7/i9510 using 32 Itanium® 2 processors 1GHz with integrated 3MB L3 cache, 128GB memory, Linux OS.

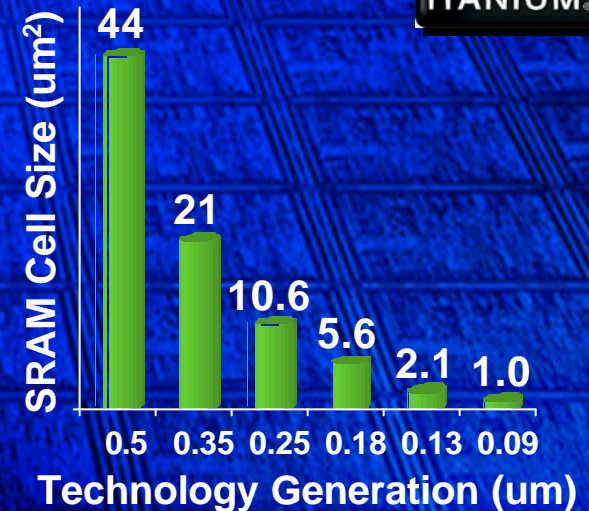
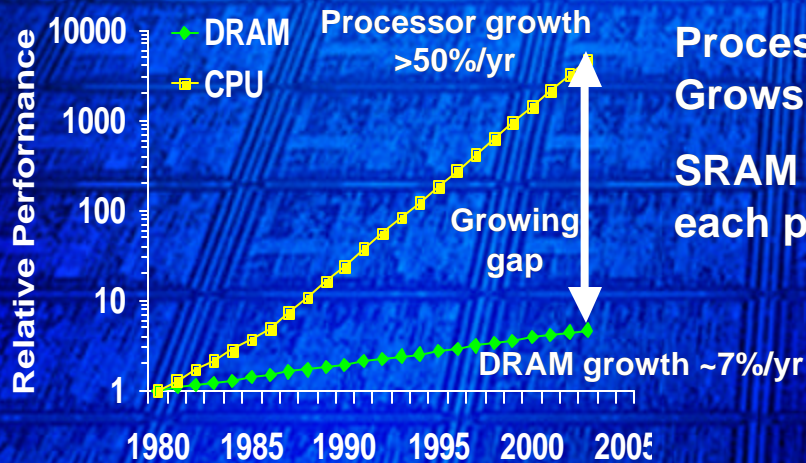
4 Source: Itanium® 2 processor measurements done on a NEC TX7/i9510 Server using 32 Itanium® 2 processors with integrated 3MB L3 cache, 256GB memory, Windows® .NET Server 2003, Datacenter Edition, Microsoft SQL Server 2000 Enterprise Edition (64bit) beta version, Availability date 12/31/02.

5 Source: Itanium® 2 processor measurements done on a SGI Scalable Linux System using 64 Itanium® 2 processors, 128GB memory, Linux OS.



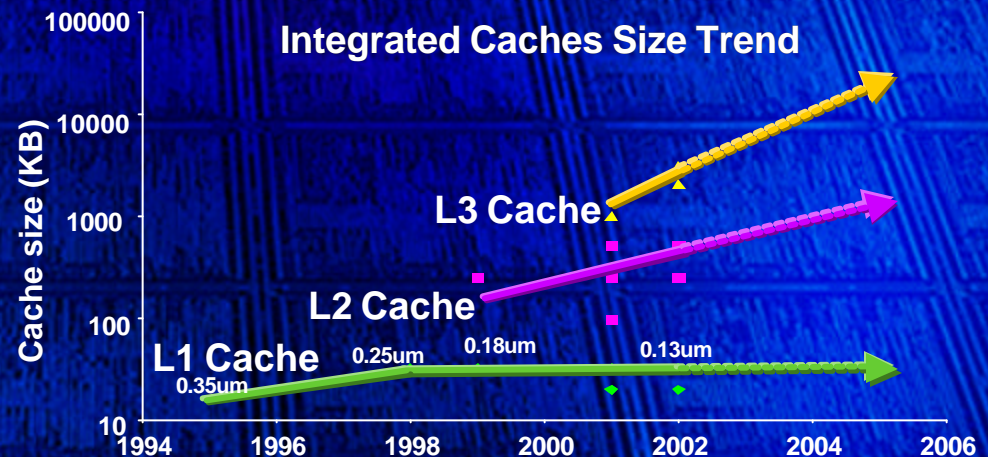
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Multi-Level Caches Reduce Memory Bottlenecks



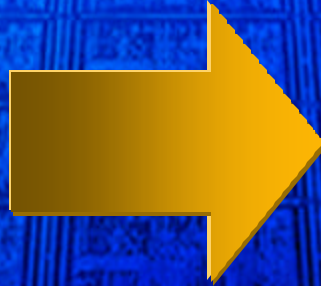
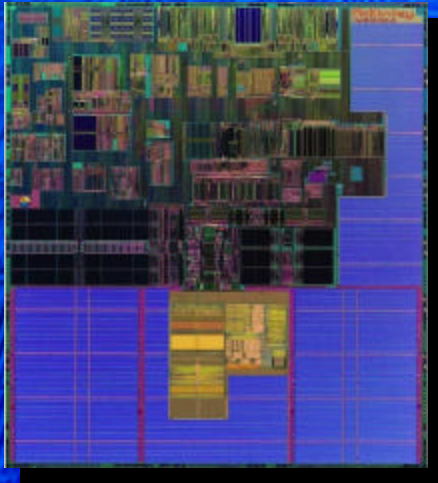
Hierarchy of caches reduce widening processor-memory gap

- Reduce average miss rates
- Reduce average memory access latency



Cache Size Will Continue To Grow

Itanium[®] 2 Processors



McKinley (0.18um)

Transistors Count Die Area



Madison (0.13um)

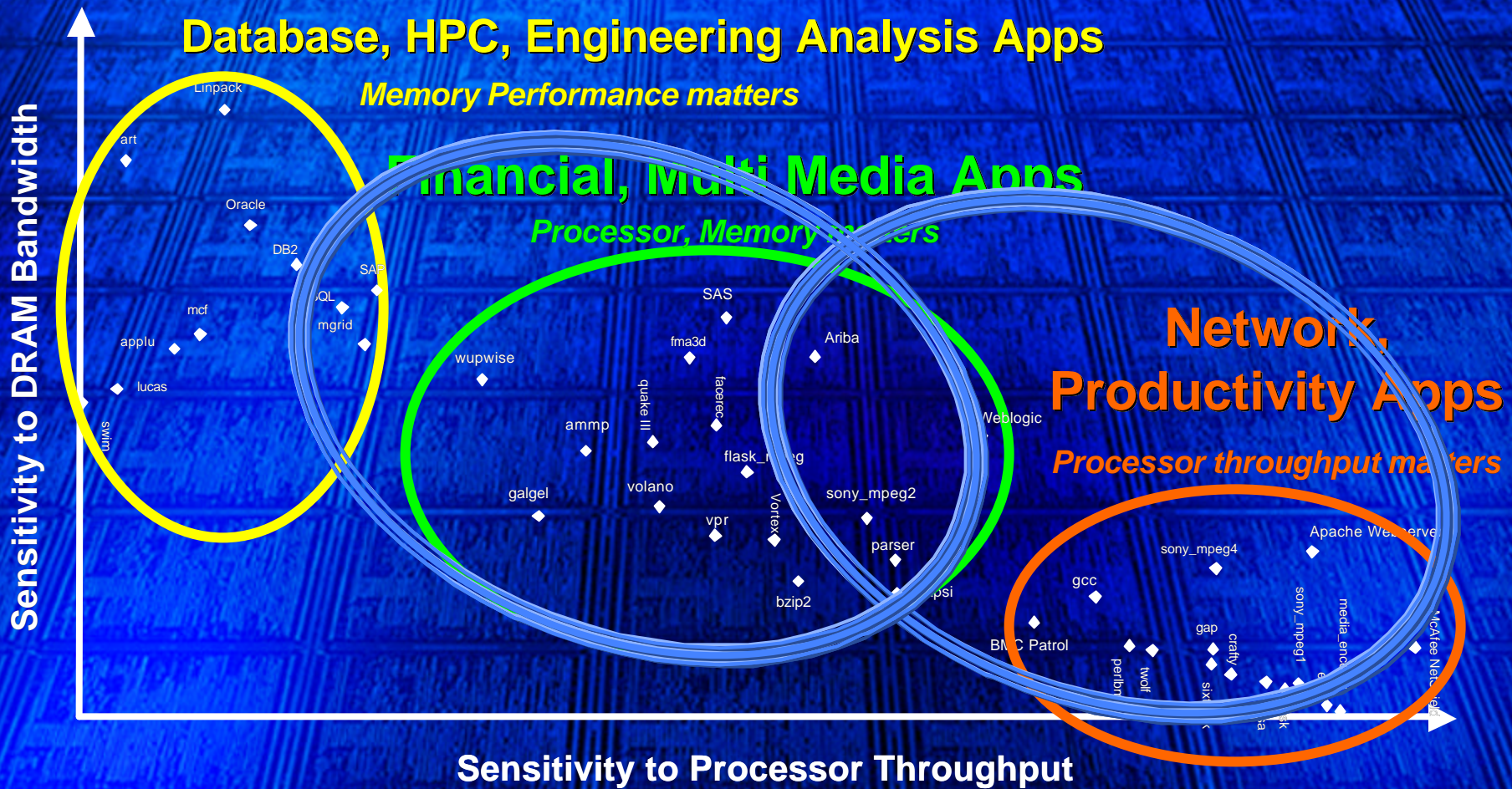
Transistors Count Die Area



**Cache Becoming An Increasing Portion Of The Die
Because Of Its Performance Impact And Low Power Density**

Xeon™ Processor Design Sweet Spots

A Snapshot

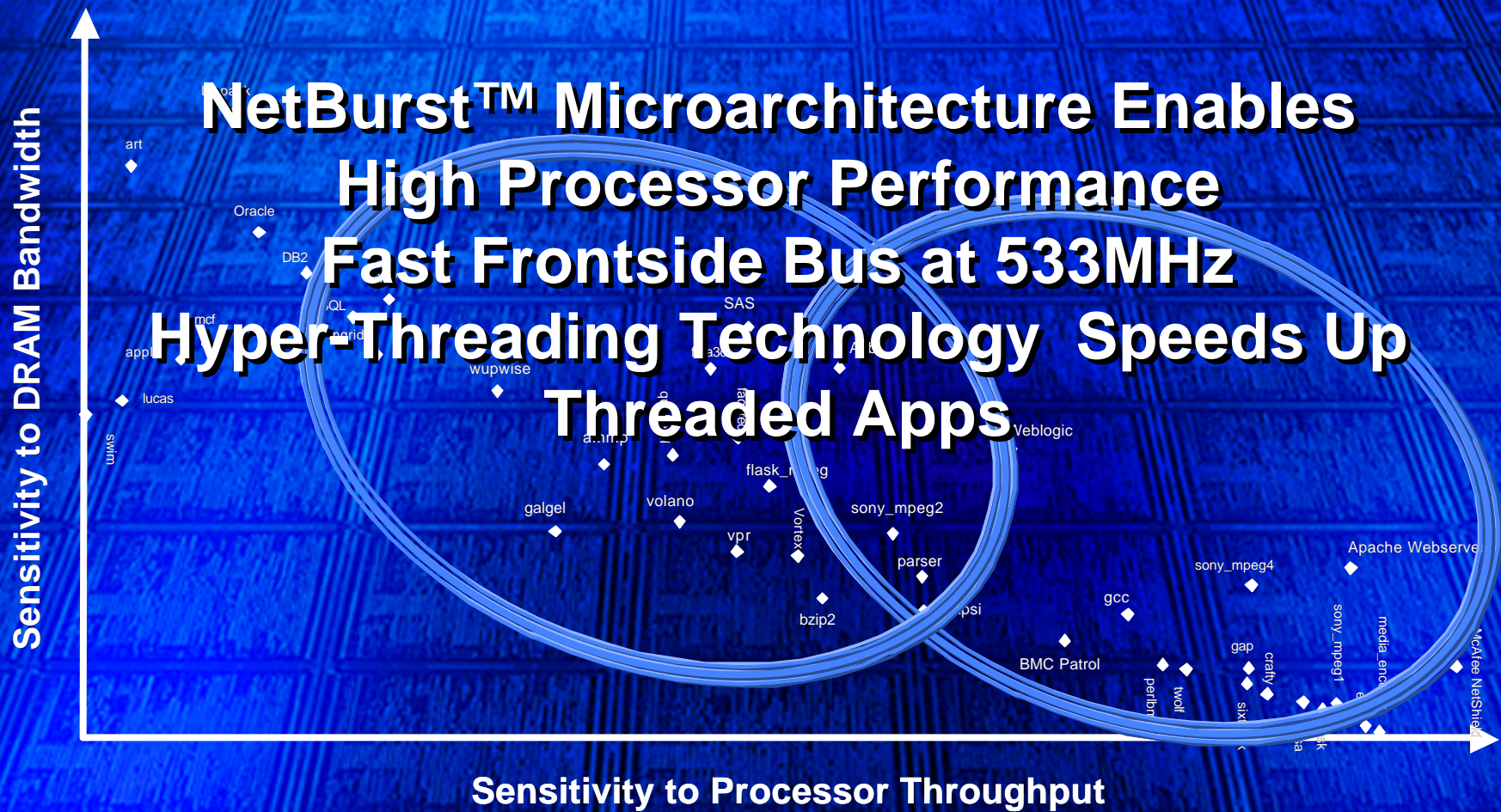


Focus: NetBurst™ μ -arch, Fast Bus, Hyper-Threading Tech.

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Xeon™ Processor Design Sweet Spots

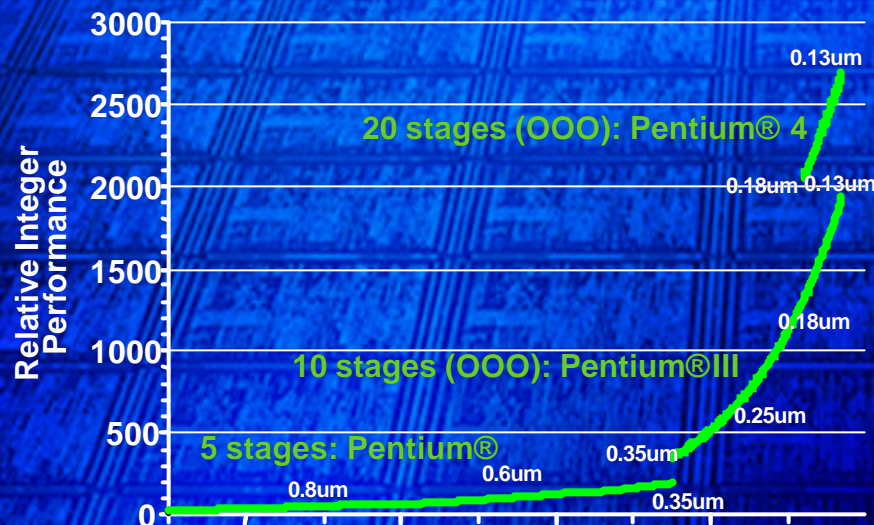
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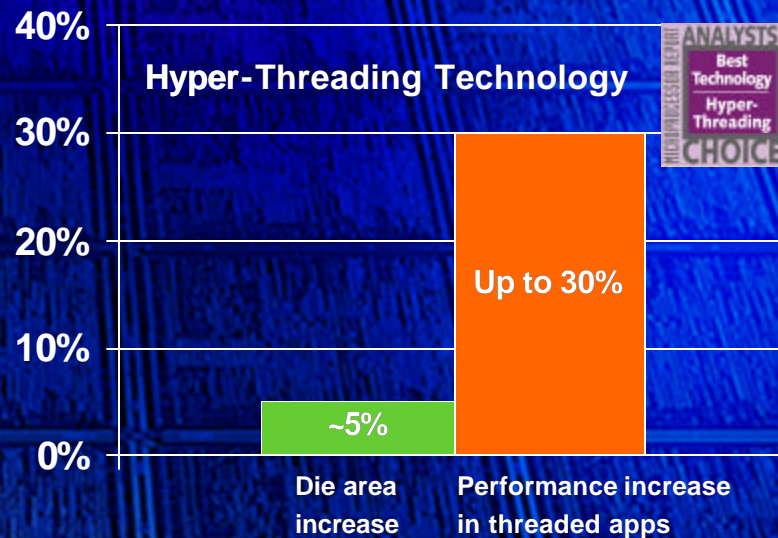
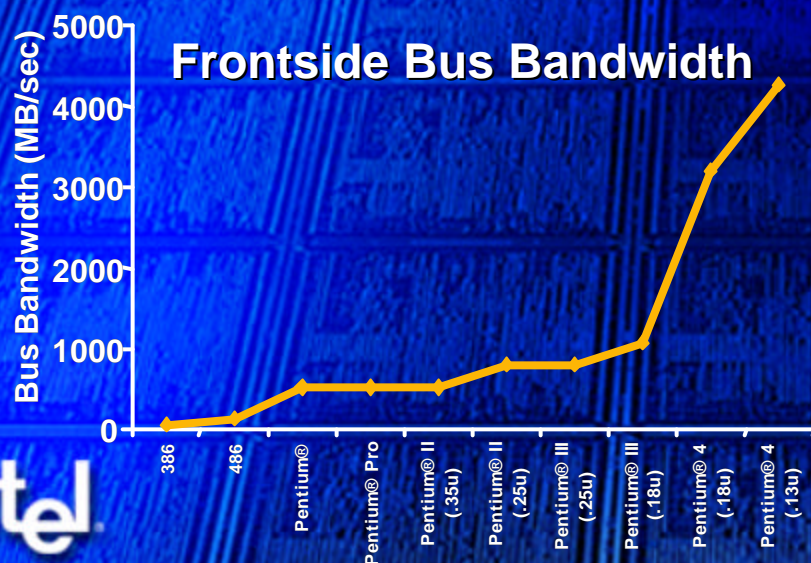
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Microarchitecture, System Bus Evolutions



- Longer pipeline enables higher throughput and frequency, resulting in greater performance
- Outstanding advances in bus bandwidth
- Hyper-Threading technology improves performance for small die cost



Summary

- Wide range of enterprise applications demand different processor and system optimizations
 - One size does not fit all
- Intel manufacturing enabled by Moore's Law drives Server innovations and performance
 - Larger caches, higher frequency, faster bus
- Intel® Itanium® and Xeon™ processor families optimized to different sweet spots for enterprise applications



Foils Available At:

http://www.intel.com/pressroom/kits/events/mpf_2002/index.htm

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